CLAIMS

1. A semiconductor device comprising:

a dicing region provided on a semiconductor substrate;

a plurality of first dummy patterns formed on a surface of the semiconductor substrate within the dicing region; and

a plurality of second dummy patterns formed above the semiconductor substrate within the dicing region so as to correspond to the plurality of first dummy patters, respectively.

2. The semiconductor device according to claim 1, wherein the plurality of first dummy patterns and the plurality of second dummy patterns are each projected.

3. The semiconductor device according to claim 1, wherein the dicing region separates a plurality of semiconductor chips from each other, the semiconductor chips each having a gate portion and being formed on the semiconductor substrate.

4. The semiconductor device according to claim 3, wherein the plurality of first dummy patterns each have a structure which is substantially similar to that of the gate portion.

5. The semiconductor device according to claim 4, wherein the plurality of first dummy patterns each have a laminated structure including a gate oxide film, a polysilicon film, a Wsi film, and a SiN film.

6. The semiconductor device according to claim 1, wherein an element isolation region having an STI structure is formed by each side of the plurality of first dummy patterns.

7. The semiconductor device according to claim 5, wherein the plurality of first dummy patterns and the element isolation regions are arranged alternately to form a repetitive pattern.

8. The semiconductor device according to claim 1, wherein the plurality of second dummy patterns are protection films provided on the semiconductor substrate.

9. The semiconductor device according to claim 1, wherein the plurality of second dummy patterns include insulation films deposited on the semiconductor substrate.

10. The semiconductor device according to claim 1, wherein the plurality of first dummy patterns and the plurality of second dummy patterns are arranged at regular intervals.

11. The semiconductor device according to claim 10, wherein the plurality of first dummy patterns and the plurality of second dummy patterns are arranged at intervals of 1.5 μm or less.

12. The semiconductor device according to claim 1, wherein the plurality of first dummy patterns and the plurality of second dummy patterns are formed along a dicing direction of the dicing region.

13. The semiconductor device according to claim 1, wherein the plurality of first dummy patterns and the plurality of second dummy patterns prevent a large waste from being caused due to a crack during a dicing operation.